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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/161,478	09/28/1998	KENJI TOYOSAWA	1035-204	7703

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EXAMINER

GRAYBILL, DAVID E

ART UNIT PAPER NUMBER

2827

DATE MAILED: 04/24/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/161,478	TOYOSAWA ET AL.	
	Examiner	Art Unit	
	David E Graybill	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 February 2002.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,2,4-11,13-19 and 23-27 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,2,4-11,13-19 and 23-27 is/are rejected.
- 7) ☒ Claim(s) 8 and 17 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) <u>3 15</u> . | 6) <input type="checkbox"/> Other: _____ |

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In the remarks entered 2-5-2 applicant requests consideration of the IDS file 10-29-1, and initialing of the IDS filed 2-22-99. Instead, the record has been revised by listing the considered reference on an attached PTO 892.

Claims 8 and 17 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claims, or amend the claims to place the claims in proper dependent form, or rewrite the claims in independent form.

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

The amendments filed 3-21-01 and 7-24-01 are objected to under 35 U.S.C. 132 because they introduce new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is the amendments to claims 1 and 10, lines 9 and 16-18; and claim 23, lines 6 and 11-13 in the amendment filed 3-21-01, and the amendments to claim 1, lines 9, 10, 18 and 19; claim 10,

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lines 10, 11, 18 and 19; and claim 23, line 13, in the amendment filed 7-24-01. To further clarify, any negative limitation or exclusionary proviso must have basis in the original disclosure. See Ex parte Grasselli, 231 USPQ 393 (Bd. App. 1983) aff'd mem., 738 F.2d 453 (Fed. Cir. 1984). The mere absence of a positive recitation is not basis for an exclusion.

Applicant is required to cancel the new matter in the reply to this Office Action.

Claims 1-19 and 23 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The non-described subject matter is the amendments to claims 1 and 10, lines 9 and 16-18; and claim 23, lines 6 and 11-13, in the amendment filed 3-21-01, and the amendments to claim 1, lines 9, 10, 18 and 19; claim 10, lines 10, 11, 18 and 19; and claim 23, line 13, in the amendment filed 7-24-01.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

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Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 5 there is insufficient antecedent basis for the language, "the semiconductor elements."

In the rejections infra, reference labels are generally recited only for the first recitation of identical claim language.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that

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was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 2, 4, 6-11, 13, 15, 16-19 and 23-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of applicant's admitted prior art and Miyamura (5441918).

At page 2, line 9 to page 16, line 8; and page 21, line 19 to page 23, line 4, applicant teaches as prior art the following:

1. A tape carrier package semiconductor device, which has a tape carrier and semiconductor elements that have been packaged on the tape carrier, said tape carrier package semiconductor device comprising: an insulating tape 102, a metal wiring pattern 107 installed on one surface of the insulating tape, the metal wiring pattern being provided on a metal-wiring-pattern side of the insulating tape, a through hole 105 that is provided in a manner so as to penetrate the insulating tape so that the insulating tape is allowed to bend, on the metal-wiring-pattern side of the tape, only a first insulating protective film 111 for insulating and covering the metal wiring pattern and the through hole at locations over and proximate the through hole,

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on a side of the insulating tape opposite the metal-wiring-pattern side, a second insulating protective film 105 for insulating and covering the through hole on the side opposite to the metal-wiring-pattern side, and resin sealing 115 peripheral portions where the metal wiring pattern and a semiconductor element 104 are connected; wherein the first and second insulating protective films are made of solder resist whose young's modulus is in the range of 5 kgf/mm² to 70 kgf/mm², and wherein on the metal-wiring-pad side of the insulating tape said first insulating protective film covers the metal wiring pattern on the metal wiring pattern side proximate the through hole.

2. The tape carrier package semiconductor device as defined in 1, wherein the solder resist forming the first and second insulating protective films has a thickness in the range of 5 μ m to 45 μ m.

4. The tape carrier package semiconductor device as defined in 1, wherein the solder resist forming the first and second insulating protective films is made of any of rubber, polyimide, epoxy, silicon and urethane solder resists.

6. The tape carrier package semiconductor device as defined in 1, wherein the first and second insulating films are made of the same material.

7. The tape carrier package semiconductor device as

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defined in 6, wherein the solder resist forming the first and second insulating protective films has a thickness in the range of 5 μm to 45 μm .

9. The tape carrier package semiconductor device as defined in 6, wherein the solder resist forming the first and second insulating protective films is made of any of rubber, polyimide, epoxy, silicon and urethane solder resists.

10. A liquid crystal panel display, which is provided with a liquid crystal panel and a tape carrier package semiconductor device having a tape carrier and semiconductor elements that have been packaged on the tape carrier so as to drive the liquid crystal panel, wherein said tape carrier comprises: an insulating tape, a metal wiring pattern installed on one surface of the insulating tape, the metal wiring pattern being provided on a metal-wiring-pattern side of the insulating tape, a through hole that is provided in a manner so as to penetrate the insulating tape so that the insulating tape is allowed to bend, on the metal-wiring-pattern side of the insulating tape, only a first insulating protective film for insulating and covering the metal wiring pattern and the through hole at locations over and proximate the through hole, on a side of the insulating tape opposite the metal-wiring-pattern side, a second insulating protective film for insulating and covering the through hole,

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and resin for sealing periphery portions at which the semiconductor device and the metal wiring pattern are connected, wherein the first and second insulating protective films are made of solder resist whose young's modulus is in the range of 5 kgf/mm² to 70 kg f/mm², and the first insulating protective film insulates and covers the metal wiring pattern proximate the through hole on the metal wiring pattern side.

11. The liquid crystal panel display as defined in 10, wherein the solder resist forming the first and second insulating protective films has a thickness in the range of 5 μ m to 45 μ m.

13. The liquid crystal panel display as defined in 10, wherein the solder resist forming the first and second insulating protective films is made of any of rubber, polyimide, epoxy, silicon and urethane solder resists.

15. The liquid crystal panel display as defined in 10, wherein the first and second insulating films are made of the same material.

16. The liquid crystal panel display as defined in 15, wherein the solder resist forming the first and second insulating protective films has a thickness in the range of 5 μ m to 45 μ m.

18. The liquid crystal panel display as defined in 15, wherein the solder resist forming the first and second insulating

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protective films is made of any of rubber, polyimide, epoxy, silicon and urethane solder resists.

23. A tape carrier package semiconductor device comprising:
an insulating tape, a metal wiring pattern on one surface of the insulating tape, the metal wiring pattern being provided on a metal-wiring-pattern side of the insulating tape
a through hole provided in a manner so as to penetrate the insulating tape so that the insulating tape is allowed to bend, on the metal-wiring-pattern side of the insulating tape, only a first insulating solder resist protective film for insulating and covering the metal wiring pattern and the through hole, and on a side of the insulating tape opposite the metal-wiring-pattern side, a second insulating solder resist protective film for insulating and covering the through hole, wherein the first and second insulating solder resist protective films are made of solder resist whose young's modulus is in the range of 5 kgf/mm² to 70 kgf/mm², and on the metal-wiring-pad side of the insulating tape said first insulating solder resist protective film covers the metal wiring pattern near the through hole on the metal wiring pattern side.

24. A tape carrier package semiconductor device, which has a tape carrier and semiconductor elements that have been packaged on the tape carrier, characterized in that said tape carrier

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comprises: an insulating tape, a metal wiring pattern installed on one surface of the insulating tape, a through hole that is provided in a manner so as to penetrate the insulating tape so that the insulating tape is allowed to bend, a first insulating protective film for insulating and covering the metal wiring pattern and the through hole on a metal-wiring-pattern side of the tape, a second insulating protective film for insulating and covering the through hole on the side opposite to the metal-wiring-pattern side, wherein the first and second insulating protective films are made of solder resist whose young's modulus is in the range of 5 kgf/mm² to 70 kgf/mm².

25. A liquid crystal panel display, which is provided with a liquid crystal panel and a tape carrier package semiconductor device having a tape carrier and semiconductor elements that have been packaged on the tape carrier so as to drive the liquid crystal panel, characterized in that said tape carrier comprises: an insulating tape, a metal wiring pattern installed on one surface of the insulating tape, a through hole that is provided in a manner so as to penetrate the insulating tape so that the insulating tape is allowed to bend, a first insulating protective film for insulating and covering the metal wiring pattern and the through hole on a

metal-wiring-pattern side of the tape, a second insulating protective film for insulating and covering the through hole on the side opposite to the metal-wiring-pattern side, wherein the first and second insulating protective films are made of solder resist whose young's modulus is in the range of 5 kgf/mm² to 70 kgf/mm².

26. A tape carrier package semiconductor device, which has a tape carrier and semiconductor elements that have been packaged on the tape carrier, characterized in that said tape carrier comprises: an insulating tape, a metal wiring pattern installed on one surface of the insulating tape, a through hole that is provided in a manner so as to penetrate the insulating tape so that the insulating tape is allowed to bend, a first insulating protective film for insulating and covering the metal wiring pattern and the through hole on a metal-wiring-pattern side of the tape, a second insulating protective film for insulating and covering the through hole on the side opposite to the metal-wiring-pattern side, wherein the first and second insulating protective films are made of solder resist whose young's modulus is in the range of 5 kgf/mm² to 70 kgf/mm², and wherein the first insulating protective film is made of solder resist of one kind.

27. A liquid crystal panel display, which is provided with a liquid crystal panel and a tape carrier package semiconductor device having a tape carrier and semiconductor elements that have been packaged on the tape carrier so as to drive the liquid crystal panel, characterized in that said tape carrier comprises:

an insulating tape, a metal wiring pattern installed on one surface of the insulating tape, a through hole that is provided in a manner so as to penetrate the insulating tape so that the insulating tape is allowed to bend, a first insulating protective film for insulating and covering the metal wiring pattern and the through hole on a metal-wiring-pattern side of the tape, a second insulating protective film for insulating and covering the through hole on the side opposite to the metal-wiring-pattern side, wherein the first and second insulating protective films are made of solder resist whose young's modulus is in the range of 5 kgf/mm² to 70 kgf/mm², and wherein the first insulating protective film 111 is made of only one kind of solder resist.

To further clarify the teaching of only a first insulating protective film 111 for insulating and covering the metal wiring pattern and the through hole at locations over and proximate the through hole, it is noted that the scope of the limitation is

limited to a film both covering the metal wiring pattern and the through hole, and only film 111 both covers the metal wiring pattern and the through hole on the metal-wiring-pattern side of the tape.

As cited, for example, at page 5, antepenultimate line to page 6, line 17, applicant also teaches as prior art a product wherein no insulating protective film other than a first polyimide insulating protective film covers the metal wiring pattern on the metal wiring pattern side proximate the through hole, no insulating solder resist other than a first polyimide insulating solder resist protective film covers the metal wiring pattern near the through hole on the metal wiring pattern side, and only a first polyimide insulating protective film insulates and covers the metal wiring pattern proximate the through hole on the metal wiring pattern side.

However, applicant does not appear to explicitly teach all of these prior art limitations in the same embodiment. Nonetheless, it would have been obvious to combine all of the limitations of the applied prior art in the same embodiment because it would provide a polyimide solder resist having desirable flexibility with fewer process steps.

In addition, applicant does not appear to explicitly teach the particular claimed panel size. Notwithstanding, it would

have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose this particular size because applicant has not disclosed that the size is for a particular unobvious purpose, produces an unexpected result, or is otherwise critical, and it appears prima facie that the product would possess utility using another dimension.

Moreover, it has been held that limitations directed to size are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Also, applicant does not appear to explicitly teach as prior art wherein the solder resist of the first and second insulating protective film includes a filler in the range of 10 wt% to 40 wt% that determines the viscosity thereof.

Nevertheless, at column 5, lines 39-51, Miyamura teaches wherein a solder resist of an insulating protective film includes a filler in the range of 10 wt% to 40 wt% that

determines the viscosity thereof. In addition, it would have been obvious to combine the product of Miyamura with the product of applicant's admitted prior art because it would provide a solder resist having desirable properties.

Claims 5 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art as applied to claims 1, 2, 4, 6-11, 13, 15, 16-19 and 23 supra, and further in combination with Kimura (5767571).

As cited, in particular at page 3, lines 20-22; and page 5, antepenultimate line to page 6, line 5, applicant teaches wherein the periphery of portions at which the tape carrier and the driving semiconductor elements have been electrically connected is covered with resin 115 having an insulating property in a manner so as to allow the edge of the resin to make an angle of not more than 70° with the upper surface of the first insulating protective film. Although applicant does not appear to literally teach as conventional the claimed resin angle, it is noted that applicant teaches this angle with reference to Fig.1(b), and the prior art figures 7(b) and 9(b) illustrate identical resin angles.

Also, applicant does not appear to explicitly teach as prior art a liquid resin. Nevertheless, at column 7, lines 1-3 and 60-65, Kimura teaches a liquid resin 5, and further teaches

wherein the periphery of portions at which a tape carrier 3 and driving semiconductor elements 1 have been electrically connected is covered with liquid resin 5 having an insulating property in a manner so as to allow the edge of the resin to make an angle of not more than 70° with the upper surface of the first insulating protective film. Moreover, it would have been obvious to combine the product of Kimura with the product of applicant's admitted prior art because it would reduce package size.

Because the publication date of applicant's admitted prior art is not disclosed, in the alternative, claims 1, 2, 4, 6-11, 13, 15, 16-19 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of applicant's admitted prior art and Miyamura (5441918), and further in combination with Tajima (5398128).

The combination of applicant's admitted prior art and Miyamura is applied as it was applied to claims 1, 2, 4, 6-11, 13, 15, 16-19 and 23 supra except for the teachings that no insulating protective film other than a first insulating protective film covers the metal wiring pattern on the metal wiring pattern side proximate the through hole, no insulating solder resist other than a first insulating solder resist protective film covers the metal wiring pattern near the through

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hole on the metal wiring pattern side, and only a first insulating protective film insulates and covers the metal wiring pattern proximate the through hole on the metal wiring pattern side.

At column 2, line 55 to column 6, line 45, Tajima teaches wherein no insulating protective film other than a first polyimide insulating protective film 6 or 7 covers a metal wiring pattern 4 on a metal wiring pattern side proximate a through hole 2, no insulating solder resist other than a first polyimide insulating solder resist protective film 6 or 7 covers the metal wiring pattern near the through hole on the metal wiring pattern side, and only a first polyimide insulating protective film 6 or 7 insulates and covers the metal wiring pattern proximate the through hole on the metal wiring pattern side. Moreover, it would have been obvious to combine the product of Tajima with the product of applicant's admitted prior art because it would provide a film.

Also, applicant does not appear to explicitly teach the particular claimed panel size. Notwithstanding, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose this particular size because applicant has not disclosed that the size is for a

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particular unobvious purpose, produces an unexpected result, or is otherwise critical, and it appears prima facie that the product would possess utility using another dimension.

Moreover, it has been held that limitations directed to size are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Also in the alternative, claims 5 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of applicant's admitted prior art and Tajima as applied to claims 1, 2, 4, 6-11, 13, 15, 16-19 and 23 supra, and further in combination with Kimura (5767571).

As cited, in particular, at page 3, lines 20-22; and page 5, antepenultimate line to page 6, line 5, applicant teaches wherein the periphery of portions at which the tape carrier and the driving semiconductor elements have been electrically connected is covered with resin 115 having an insulating property in a manner so as to allow the edge of the resin to

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make an angle of not more than 70° with the upper surface of the first insulating protective film. Although applicant does not appear to literally teach as conventional the claimed resin angle, it is noted that applicant teaches this angle with reference to Fig.1(b), and the prior art figures 7(b) and 9(b) illustrate identical resin angles.

Also, applicant does not appear to explicitly teach as prior art a liquid resin. Nevertheless, at column 7, lines 1-3 and 60-65, Kimura teaches a liquid resin 5, and further teaches wherein the periphery of portions at which a tape carrier 3 and driving semiconductor elements 1 have been electrically connected is covered with liquid resin 5 having an insulating property in a manner so as to allow the edge of the resin to make an angle of not more than 70° with the upper surface of the first insulating protective film. Moreover, it would have been obvious to combine the product of Kimura with the product of the applied prior art because it would reduce package size.

Applicant's amendment and remarks filed 2-5-2 are addressed in the rejection supra and elsewhere in the record, and are further addressed infra.

Applicant traverses the objection to the amendments filed 3-21-01 and 7-24-01 under 35 U.S.C. 132, and the rejection of claims 1-19 and 23 under 35 U.S.C. 112, first paragraph.

In particular, applicant argues that Fig.1(b) provides support for the negative limitations. This argument is respectfully traversed because, at best, Fig.1(b) provides support only for a positive limitation of one film and not for a negative limitation of "only" one film. Specifically, in Fig.1(b) there is merely an absence of a positive illustration of other than a first insulating protective film for insulating and covering the metal wiring pattern and the through hole on the metal-wiring-pattern side, at locations over and proximate the through hole, wherein no insulating protective film other than the first insulating protective film covers the metal wiring pattern on the metal wiring pattern side proximate the through hole, and other than the first insulating protective film insulates and covers the metal wiring pattern proximate the through hole on the metal wiring pattern side. As explicitly stated in the rejection, "The mere absence of a positive recitation is not basis for an exclusion." To further clarify, in Fig.1(b) there is also an absence of a positive illustration of elements 11 and 12 which are illustrated in Fig.4(c); yet, as evidenced by Fig.4(c), there would be no more support in Fig.1(b) for a negative limitation in the claims excluding elements 11 and 12, than there is for the instant negative limitations.

Relatedly, applicant cites the instant specification, page 41, lines 19+, as support for the negative limitations. It is respectfully submitted that this citation provides support only for a disclosure of a process wherein "the formation of the solder resist is made only once," and not for the product limitations, "only a first insulating protective film for insulating and covering the metal wiring pattern and the through hole on the metal-wiring-pattern side, at locations over and proximate the through hole," and, "wherein no insulating protective film other than said first insulating protective film covers the metal wiring pattern on the metal wiring pattern side proximate the through hole," and, "only the first insulating protective film insulates and covers the metal wiring pattern proximate the through hole on the metal wiring pattern side."

In addition, applicant argues that the claimed invention yields unexpected results. This argument is respectfully deemed to be unpersuasive because the original disclosure merely evidences results obtained by routine experimentation and optimization, and does not disclose unexpected results. In any case, it is respectfully submitted that unexpected results must be established by factual evidence, and not by mere argument. See, for example, *In re De Blauwe*, 736 F.2d 699, 222 USPQ 191, 196 (Fed. Cir. 1984). To this end, the arguments of counsel

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cannot take the place of evidence in the record. In re Schulze, 346 F.2d 600, 602, 145 USPQ 716, 718 (CCPA 1965). Instead, the evidence relied on should establish "that the differences in results are in fact unexpected and unobvious and of both statistical and practical significance." Ex parte Gelles, 22 USPQ2d 1318, 1319 (Bd. Pat. App. & Inter. 1992). See also, Ex parte C, 27 USPQ2d 1492 (Bd. Pat. App. & Inter. 1992); In re Nolan, 553 F.2d 1261, 193 USPQ 641, 645 (CCPA 1977); and In re Eli Lilly, 902 F.2d 943, 14 USPQ2d 1741 (Fed. Cir. 1990).

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).


A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

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Any telephone inquiry of a general nature or relating to the status (MPEP 203.08) of this application or proceeding should be directed to the group receptionist whose telephone number is 703-308-1782.

Any telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (703) 308-2947. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.

The fax phone number for group 2800 is 703/305-3431.



David E. Graybill
Primary Examiner
Art Unit 2827

D.G.
18-Apr-02